



UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,670	11/21/2003	Yoichi Endo	100353-00180	9063

4372 7590 12/23/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER

MISIURA, BRIAN THOMAS

ART UNIT	PAPER NUMBER
----------	--------------

2112

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/717,670	Applicant(s) ENDO ET AL.	
	Examiner Brian T. Misiura	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,10,12 and 17 is/are rejected.
- 7) ☒ Claim(s) 2,4-9,11 and 13-16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whipple, U.S. PN. 5,077,733 in view of Ayukawa et al. U.S. PN 6,697,906.

1. As per Claim 1, Whipple discloses a shared bus system, comprising:
 - a bus; (column 2, line 27)
 - a first circuit coupled to said bus to access said bus (column 2 lines 32-33)
 - a second circuit coupled to said bus to share said bus with said first circuit, and to access said bus; (column 2, lines 32-33)
 - a counter circuit, which is provided in said second circuit, and performs a counting operation each time said second circuit accesses said bus; (column 21 lines 36-39, and Abstract lines 8-15)

Art Unit: 2112

- wherein said second circuit releases the right to use said bus in response to detection of a predetermined number of counting operations performed by said counter circuit (abstract, lines 8-15)

Whipple does not disclose:

- an arbiter circuit coupled to said bus, said first circuit, and said second circuit to receive requests for a right to use said bus from said first circuit and said second circuit and to arbitrate the requests between said first circuit and said second circuit
- after acquiring the right to use said bus from said arbiter circuit

However, Ayukawa et al. discloses:

- an arbiter circuit coupled to said bus (figure 1 numeral 17), said first circuit (figure 1 numeral 26), and said second circuit (figure 1 numeral 27) to receive requests for a right to use said bus from said first circuit and said second circuit and to arbitrate the requests between said first circuit and said second circuit (column 4 lines 1-5, figure 1)
- after acquiring the right to use said bus from said arbiter circuit (column 4, lines 1-5 figure 1)

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Ayukawa into the system of Whipple to provide a way to sort through bus requests and select a requesting device to be granted the right to use the bus.

- The modification would have been obvious because one having ordinary skill in the art would want to provide a way to sort through bus requests and select a requesting device to be granted the right to use the bus (Ayukawa, column 4 lines 1-5, figure 1).

Art Unit: 2112

2. As per claim 3, Whipple discloses the system wherein a second circuit includes a register circuit, and the predetermined number is equal to a value stored in said register circuit (column 21, lines 54-60).

3. As per claim 10, Whipple discloses a method of sharing a bus, comprising the steps of:

- counting a number of accesses made to the shared bus after acquiring the right to use the shared bus (column 23, lines 14-16);
- releasing the shared bus in response to an event that the number of accesses reaches a predetermined number (claim 15, column 25, lines 11-12).

Whipple does not disclose:

- sending to an arbiter circuit a request to grant a right to use a shared bus;
- arbitrating at the arbiter circuit if a plurality of requests for the right to use the shared bus are made;
- acquiring the right to use the shared bus from the arbiter circuit in response to the request;

However, Ayukawa et al. discloses:

- sending to an arbiter circuit a request to grant a right to use a shared bus (column 4 lines 1-5, figure 1);
- arbitrating at the arbiter circuit if a plurality of requests for the right to use the shared bus are made (column 4 lines 1-5, figure 1);
- acquiring the right to use the shared bus from the arbiter circuit in response to the request (column 4, lines 1-5, figure 1);

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Ayukawa into the system

Art Unit: 2112

of Whipple to provide a way to sort through bus requests and select a requesting device to be granted the right to use the bus.

- The modification would have been obvious because one having ordinary skill in the art would want to provide a way to sort through bus requests and select a requesting device to be granted the right to use the bus (Ayukawa, column 4 lines 1-5, figure 1).

4. As per claim 12, Whipple discloses a method further comprising a step of storing a value in a register circuit, and the predetermined number is equal to the value stored in said register circuit. (column 21, lines 54-60)

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Whipple, U.S. Patent No. 5,077,733, in view of Ayukawa et al. U.S. PN 6,697,906, in further view of Takita et al, U.S. Patent No. 5,684,505.

6. As Per claim 17, Whipple and Ayukawa do not disclose a method wherein a bus is a memory bus to which a memory is connected, and a memory interface for accessing a memory through a memory bus shares a memory bus together with a liquid crystal display controlling circuit for controlling driving of a liquid crystal display device through said memory bus.

However Takita discloses a memory bus, display controller and a liquid crystal display device (Takita, column 38, lines 60-65).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Whipple, Ayukawa, and Takita.

One of ordinary skill would be motivated to use a liquid crystal display since such a type of device has been quite a well-known type of display device in prior existing art.

Allowable Subject Matter

Claims 2, 4-9, 11, and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

Applicant's amendment filed on 11/10/2005 has been fully considered but do not place the application in condition for allowance.

Response to Arguments

1. In the applicant's amendments, the applicant states that *Whipple* fails to teach "the right to use the bus that is released after a predetermined number of accesses", as recited by amended Claim 1. The applicant states that the right to use the bus that is disclosed in the application is different than the highest priority disclosed in *Whipple*.

With regards to this limitation of amended Claim 1, *Whipple* discloses in column 1, lines 19-27,

The present invention relates to apparatus used in computer systems to determine which of a plurality of devices which share a bus is to **have access to the bus at a given instant...** Therefore, the node that currently has the highest priority, anchor node, is "granted a programmable number of bus accesses before relinquishing the highest priority to another device." Further defining highest priority, *Whipple* discloses in column 1 lines 33-36; "if a device with a high priority and one with a low priority both attempt to access the bus, the device with the higher priority wins." This further establishes that a node with the highest priority also has the right to use the bus.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Misiura

Rehana Perveen
REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/20/05